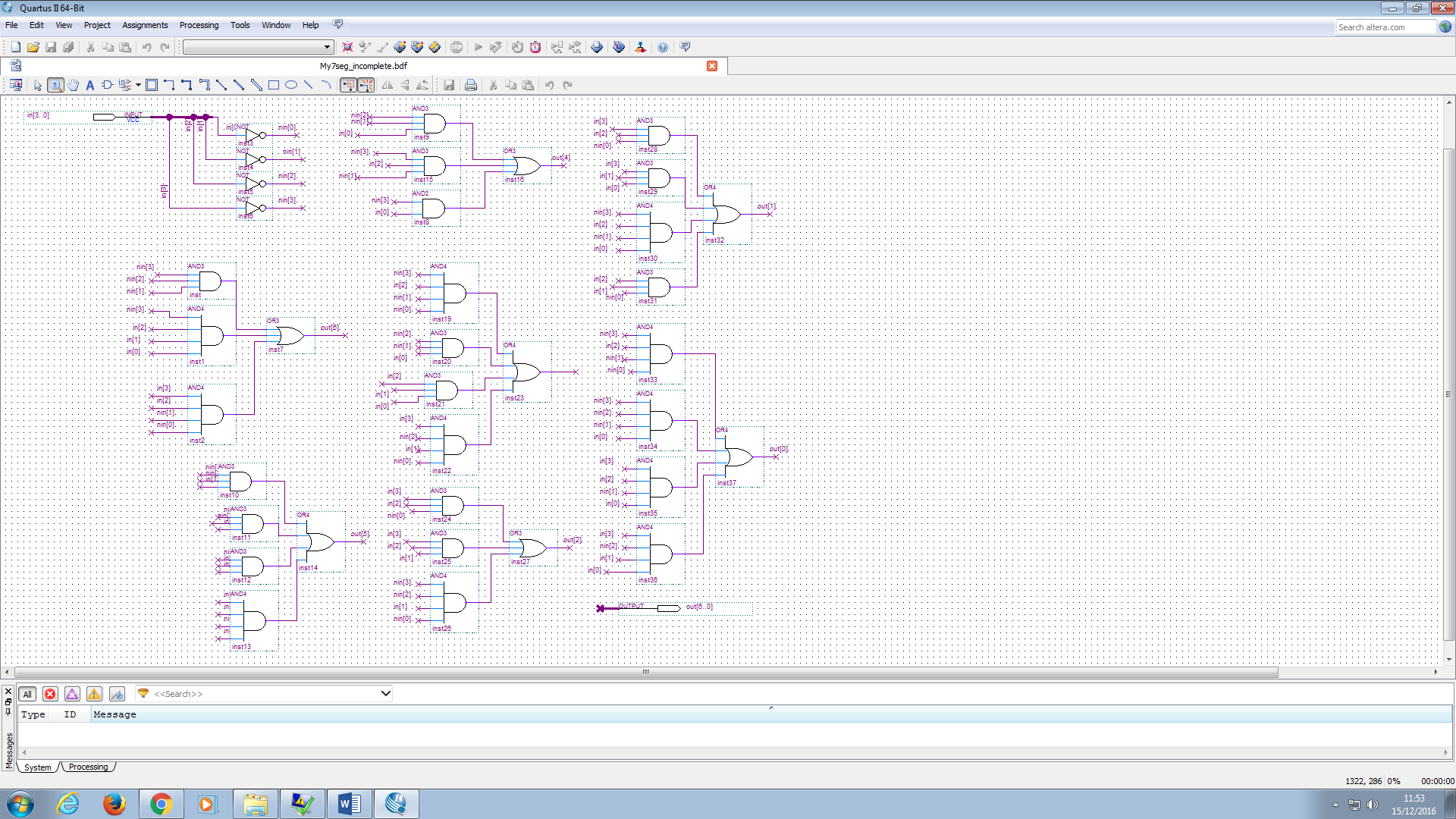
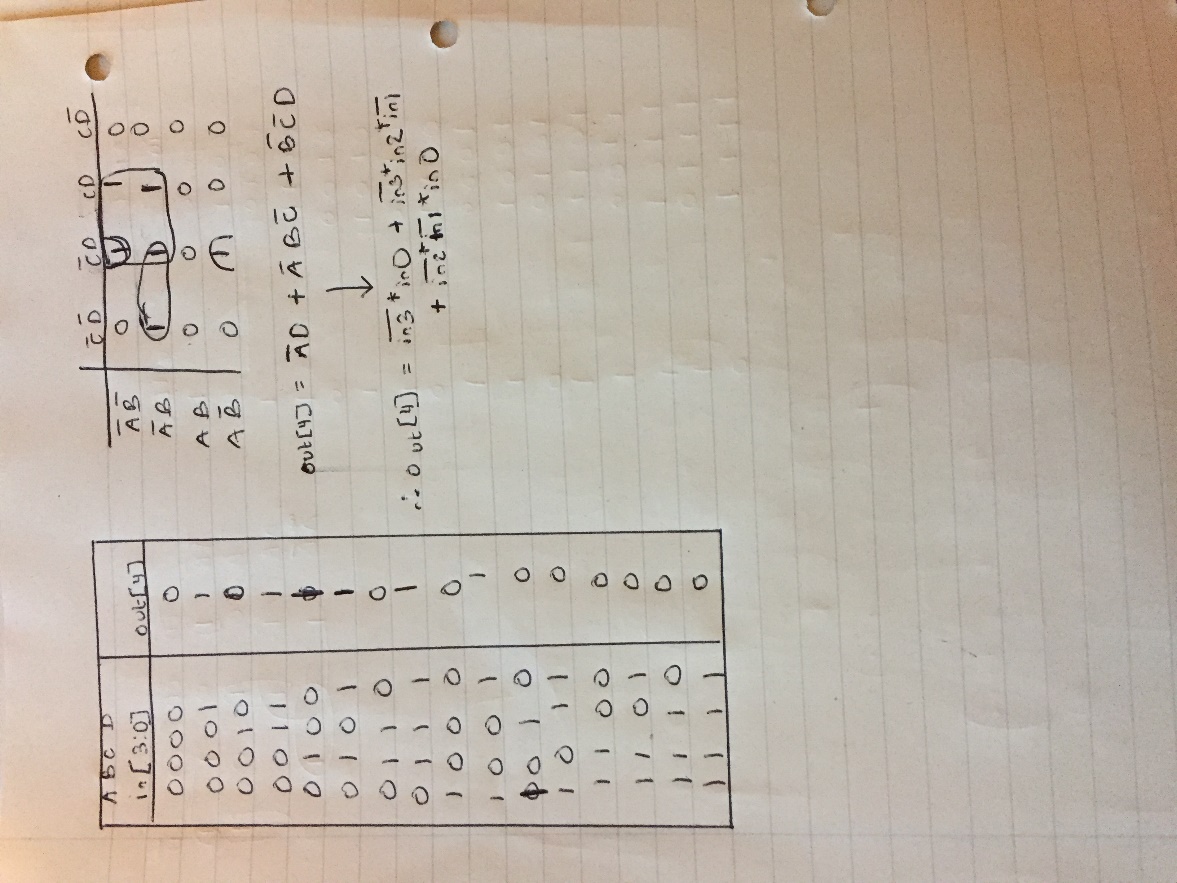
Verilog Experiment - Part 1

Experiment 1 – Schematic Capture for 7 Segment Display

Figure 1 - Entire Schematic Diagram for 7-Segment Decoder

On the left is the derivation for output 4 of the 7-Segment decoder which is boxed in red in Figure 1.

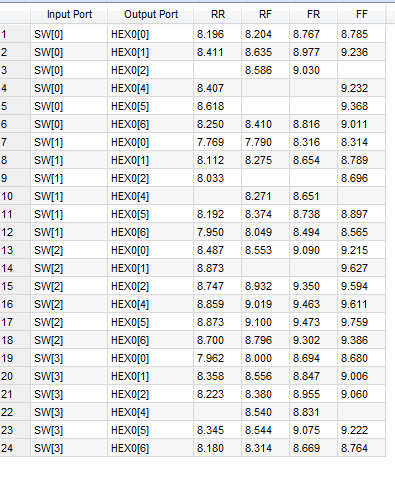
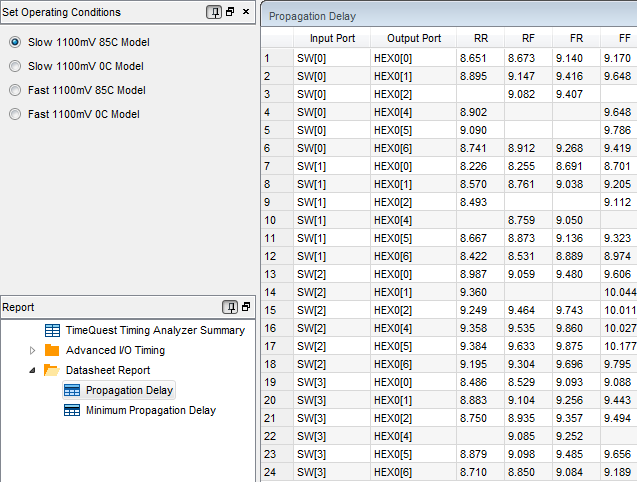
Figure 2A – Slow 0C 1100mv Model Figure 2B – Slow 85C 1100mv Model

Figure 2 shows the worst-case input to output propagation delays for various combinations of rise and fall times and two temperature extremes.

RR – input rising, output rising

RF – input rising, output falling

FR – input falling, output rising

FF – output falling, input falling

There are some gaps in the table for certain combinations due to some of the circuit logic. For example, a buffer has either RR or FF and cannot have FR or RF. On the other hand, an inverter can have RF or FR and cannot have RR or FF.

There are propagation delays due to parasitic capacitance in the transistors as it takes time for them to charge and discharge.

Propagation delay can be approximated using the RC constant. So at higher temperatures, the resistance increases, so RC increases which relates to a higher propagation delay at higher temperatures as shown in the above figure. Temperature also affects material properties such as threshold voltage and other parameters which also affect propagation delay time.

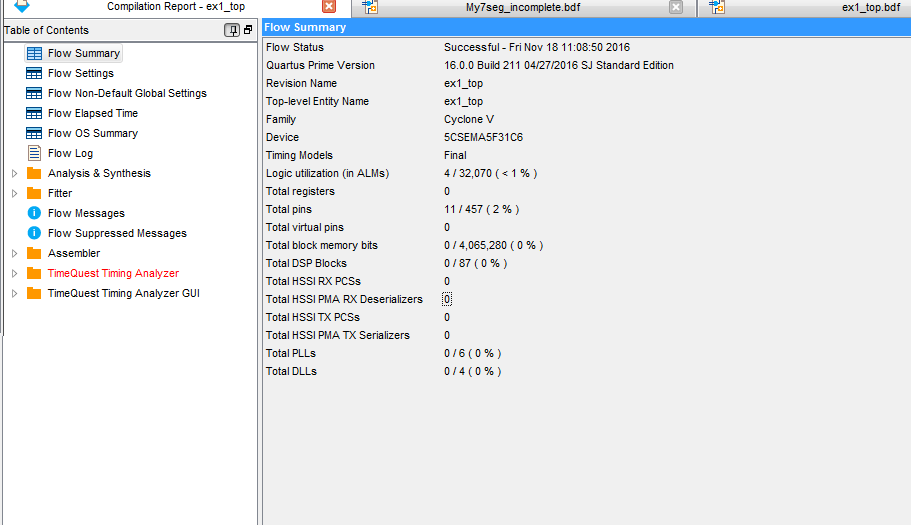
Figure 3 shows that only a small number of resources are used. In this case 4 ALMs and 11 pins

Figure 3 – Compilation Report